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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,678	09/21/1999	DUANE L. ABBEY	98CR023/KE	2540

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ATTENTION: KYLE EPPELE
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EXAMINER	
MUNOZ, GUILLERMO	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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Office Action Summary	Application No.	Applicant(s)
	09/399,678	ABBEY, DUANE L.
	Examiner	**Art Unit**
	Guillermo Munoz	2634

-- ***The MAILING DATE of this communication appears on the cover sheet with the correspondence address*** --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 21 September 1999 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,13,14,16-26 and 29 is/are rejected.

7)☒ Claim(s) 9-12, 15, 27, 28, and 30 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 September 1999 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 13, 14, 16-26, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al ("High Speed Polyphase CIC Decimation Filter", Circuits and Systems, 12-15 May 1996. ISCAS '96, 'Connecting the World', 1996 IEEE International Symposium, VOL. 2, pages 229-232) in view of Hogenauer, Eugene B. ("An Economical Class of Digital Filters for Decimation and Interpolation", April 1981. IEEE Transactions on Acoustics, Speech, and Signal Processing. VOL. ASSP-29, NO. 2) and Gao et al ("A Partial-Polyphase VLSI Architecture for Very High Speed CIC Decimation Filters", 1999. Proceedings. Twelfth Annual IEEE International, 1999, Pages 391-395).

In regards to claims 1 and 26; Yang et al teaches a polyphase CIC decimation filter wherein:

- "Hogenauer's CIC decimation filter [5], shown in Fig. 1, consists of N cascaded digital integrators operating at a high input sampling rate, f_s, and N cascaded differentiators at a low rate, f_s/R, were R is the integer downconversion factor"(page 229, col.1, Fig.1)
- "Instead of using one CIC filter to decimate the high speed digital signal, here we use two (one N_1-stage and one N_2-stage). The downconversion factors for them are R_1 and R_2, respectively. Here we assume that R can be factored as $R_1 * R_2$"(page 230, col.3).

- "Where $F_i(z)$ are polyphase components, operating at the rate of f_s/R_1. Thus the polyphase structure for CIC decimation filters can be built as shown in Fig. 2"(page 230, col.4, Fig.2).

Yang discloses that R is the product of $R_1 * R_2$, where R_1 and R_2 are decimation factors dispersed within a polyphase CIC filter. Yang, further, teaches that R_2 can be located between two comb stages. However, Yang fails to teach the need to have multiple decimation stages within a CIC filter.

Hogenauer teaches a CIC decimation filter wherein:

- "The integrator section of CIC filters consists of N ideal digital integrator stages operating at the high sampling rate, f_s"(page 155, col.2).
- "The section operates at the low sampling rate f_s/R where R is the integer rate change factor. This section consists of N comb stages with a differential delay of M samples per stage"(page 155, col.2).
- "There is a rate change switch between the two filter sections. For decimation, the switch subsamples the output of the last integrator stage, reducing the sampling rate from f_s to f_s/R"(page 156, col.3).
- "The same filter design can easily be used for a wide range of rate change factors, R, with the addition of a scaling circuit and minimal changes to the filter timing"(page 156, col.4).
- "intermediate storage is reduced by integrating at the high sampling rate and comb filtering at the low sampling rate"(page156, col.3)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to decimate the sample rate of the CIC decimation filter of Yang within the cascaded comb structure in view of Hogenauer for the purpose of achieving a desired frequency characteristic.

In regards to claim 2; as applied to claim 1 above, Yang teaches a polyphase CIC decimation filter wherein:

- "implementation of digital downconversion (or decimation)"(page 229, col.1)

The decimation of the input sampling rate f_s is equivalent to claimed first rate change component subsamples output received from said cascaded integrator structure and outputs a reduced rate signal to said cascaded comb structure in claim 2, lines 2-4.

In regards to claims 3, and 14; as applied to claims 1, and 13, respectively, Hogenauer teaches a CIC filter wherein:

- "The integrator section of CIC filters consists of N ideal digital integrator stages operating at the high sampling rate, f_s"(page 155, col.2).

The N ideal digital integrator stages are equivalent to claimed cascaded integrator structure comprises a plurality of integrator stages in claim 3 and 14.

In regards to claim 4; as applied to claim 1 above, Yang teaches a polyphase CIC filter wherein:

- "Instead of using one CIC filter to decimate the high speed digital signal, here we use two (one N_1-stage and one N_2-stage). The downconversion factors for them are R_1 and R_2, respectively. Here we assume that R can be factored as $R_1 * R_2$"(page 230, col.3).

The downconversion factor R_1 is equivalent to claimed third rate change component in claim 4.

In regards to claim 5; as applied to claim 1 above, Yang teaches a polyphase CIC filter wherein:

- "Low frequency decimators are used to further downconvert the sampling rate"(page 231, col.6).

The Low frequency decimators are equivalent to claimed plurality of additional rate change components in claim 5.

In regards to claim 6; as applied to claim 1 above, Yang teaches a polyphase CIC filter wherein:

- "Generally speaking, the higher the first downconversion rate, f_s/R, relative to the Nyquist rate, f_N, the smaller the droop"(page 229, col.2).
- "Fig. 3 for the aliasing attenuation versus intermediate oversampling ratio, IOSR = $(f_s/R_1)/f_N$"(page 230, col.4).
- "We can choose N_1=2 for IOSR $\geq$ 50"(page230, col.4).

The input signal f_s is equivalent to claimed oversampled signal as input to the cascaded integrator structure in claim 6.

In regards to claim 7; as applied to claim 6 above, Yang teaches a polyphase CIC filter wherein:

- "The time-interleaved $\Delta\Sigma$ modulators were presented in [11] and were intended for very high frequency applications"(page 232, col.8).

The $\Delta\Sigma$ modulators are equivalent to claimed delta-sigma modulator in claim 7.

In regards to claims 8 and 29; as applied to claims 1 and 26, respectively, Yang teaches a CIC filter wherein:

- "Hogenauer's CIC decimation filter [5], shown in Fig. 1, consists of N cascaded digital integrators operating at a high input sampling rate, f_s, and N cascaded differentiators at a low rate, f_s/R, were R is the integer downconversion factor"(page 229, col.1, Fig.1)

The N digital integrator stages equal the N differentiator stages, equivalent to claimed plurality of integrator stages and plurality of comb stages having an equivalent number of stages in claim 8. The N differentiator stages is equivalent to claimed cascaded comb means comprising a plurality of comb stages in claim 29.

In regards to claims 13 and 20; as applied to claim 1 above, Yang teaches a polyphase CIC filter wherein:

- "Instead of using one CIC filter to decimate the high speed digital signal, here we use two (one N_1-stage and one N_2-stage). The downconversion factors for them are R_1 and R_2, respectively. Here we assume that R can be factored as $R_1 * R_2$"(page 230, col.3).
- "Where $F_i(z)$ are polyphase components, operating at the rate of f_s/R_1. Thus the polyphase structure for CIC decimation filters can be built as shown in Fig. 2"(page 230, col.4, Fig.2).

Yang teaches that the polyphase components $F_i(z)$ operate at a downconverted rate f_s/R_1. R_1 is equivalent to claimed data rate change component establishing the data rate input to the integrator structure. Yang, also, teaches that $R=R_1*R_2$. Yang, however, fails to teach that the CIC decimator filter outputs data equivalent to a post-decimated integrator filter.

Gao et al teaches a partial polyphase CIC decimator filter wherein:

- "filters can operate at much lower sampling rate meanwhile achieve the same performance as Hogenauer's CIC filters"(page 392, col.3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to downconvert the sample rate f_s of Yang prior to input into the integrator stage in view of Gao for the purpose of operating at a lower sampling rate.

In regards to claims 16 and 22; as applied to claims 13 and 22, respectively, Gao teaches a partially polyphase CIC decimator filter wherein:

- "From Table II it's clearly seen that the polyphase decomposition is simple when filter order k and decimation ratio N_{pp} are low"

Polyphase decomposition is equivalent to claimed serial to parallel conversion in claim 16 and claimed converting a received serial data stream to a parallel signal having a plurality of parallel paths in claim 22, lines 2-3.

In regards to claims 17, 18, 23, and 24; as applied to claims 13 and 20, Yang teaches a CIC decimator filter wherein:

- "Since there are finite combinations for the polyphase components' output, a look-up table ROM can be used to store all the possible results which will be addressed by bandpass $\Delta\Sigma$ modulator's outputs "(page 231, col.5).

The ROM look-up table is equivalent to claimed read only memory device in claim 17; claimed look-up table which stores coefficients for modifying data received from data rate change component in claim 18; and claimed accessing a memory device in claim 24, line 2. The results stored in the look-up table ROM are equivalent to claimed

coefficients used to modify the received data by multiplication in claim 23 and claimed data held by said memory device being used during step to modify data received from said data rate change component.

In regards to claims 19 and 21; as applied to claims 13 and 20, respectively, Yang teaches a polyphase CIC decimator filter wherein:

- "where $F_i(z)$ are polyphase components"(page 230, col.4, Fig.2)

The multiple $F_I(Z)$ paths are equivalent to claimed plurality of reduced rate parallel signal paths with an integrator stage and a plurality of coefficient multipliers for each path in claim 19 and processing received data with a plurality of parallel integrator stages in claim 21.

In regards to claim 25; as applied to claim 20 above, Yang teaches a polyphase CIC decimator filter wherein:

- "the polyphase structure for CIC decimation filters can be built as shown in Fig.2"(page 230, col.4).

Figure 2 of the polyphase structure includes a combining stage immediately following the plurality of integration paths. The combing stage is equivalent to claimed combining procedure further modifying data received at the changed data rate in claim 25.

Claim Objections

Claims 9-12, 15, 27, 28, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (7.6).

The following patents are cited to further show the state of the art with respect to trellis coded receivers in general:

U.S. Pat. No. 2002/0034272 to Freidhof et al

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 703-305-4224. The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9313 for regular communications and 703-872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Guillermo Munoz

GM
January 27, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
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